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| HAMILTON & TERRILE, LLP P.O. BOX 203518 AUSTIN, TX 78720 | | | EXAMINER RAMPURIA, SATISH | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/002,238

Applicant(s)

WANG, FU-HWA

Examiner

Satish S. Rampuria

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-12 and 14-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-12 and 14-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Response to Amendment

1. This action is in response to the Amendment received on Feb 02, 2006.
2. Claims previously cancelled by the applicant: 6 and 13
3. Claims previously amended by the applicant: 1, 8, 16, 21, 26, 31, and 36.
4. Claims pending in the application: 1-5, 7-12, and 14-40.

Response to Arguments

5. Applicant's arguments with respect to claims have been considered but they are not persuasive.

In the remarks, the applicant has argued that:

In general, Chen, Zucker and Huang do not disclose or suggest method of producing a binary code file where the binary code file includes binary code instruction and *compiler annotation* where the *compiler annotation* is an *ELF section*, as substantially required by each of the independent claims. The ELF header 64 of Zucker neither teaches nor suggests the claimed binary code file having both binary code instructions and compiler annotation which is an ELF section. Additionally, "debugging data" as set forth by Huang neither teaches nor suggests the claimed compiler annotation.

Examiner's response:

In response to Applicants arguments, it is noted that the rejection clearly points out where Chen, Zucker and Huang teach the claimed features and why it would have been obvious to combine their teachings (see rejection below). Specifically, the rejection points out where the limitations of the claim are taught by the references Chen, Zucker and Huang. In addition, Huang discloses the limitation compiler annotation is an ELF section as being debugging data. Because compiler annotations are nothing but the information useful for binary translators as indicated by the Applicants in the Remarks, page 9. Further, Applicant presented the similar

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arguments for claim 8, 16, 21, 26, 31, and 36 are given the same reasoning as above. Therefore, the rejection is proper and maintained herein.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

7. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1, 2, 3, 5, 8, 9, 10, 12, 16, 17, 18, 20-23 25-28, and 30-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,625,807 to Chen (hereinafter called

Chen) in view of US Patent No. 5,991,871 to Zucker (hereinafter called Zucker) and further in view of the document published on the Internet

(www.cs.ucdavis.edu/~haungs/paper/node10.html) on 9/21/1998 by Michael L. Haungs (hereinafter called Haungs).

Per claims 1, 8 and 16:

Chen disclose:

- A method of producing a binary code file (col. 6, lines 40-41 “The original binary program code... generated by the system compiler”) comprising:
- compiling a plurality of source code instructions (col. 6, lines 25-26 “The original source code... is input into the system compiler”); and
- outputting a plurality of binary code instructions (col. 5, lines 47-49 “transforms the code into equivalent machine code in a form of a relocatable... or directly executable object code”) and compiler annotation (col. 6, lines 34-38 “The register usage annotator 70 generates bit vector annotation... of the system compiler 60”).

Chen does not explicitly disclose the plurality of binary code instructions being executable by a processor of a computer system, the plurality of binary code instructions are an executable and linking format (ELF) binary code file.

However, Zucker discloses in an analogous computer system the plurality of binary code instructions being executable by a processor of a computer system, the plurality of binary code instructions are an executable and linking format (ELF) binary code file (col. 8, lines 28-39 “object program 60 comprises an ELF header 64 that specifies the number and sizes of the

sections of the program 60... the operating system 48. A section header table 66 is also provided, including information required to locate all of the sections of the file 60... data of the program are provided... dynamic linking information...linker” also, FIG. 4 and related discussion).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of the plurality of binary code instructions being executable by a processor of a computer system, the plurality of binary code instructions are an executable and linking format (ELF) binary code file and the compiler annotation is an ELF section as taught by Zucker into the method of generating binary code file as taught by Chen. The modification would be obvious because of one of ordinary skill in the art would be motivated use the ELF format file to provide an application binary interface and memory mapping system that can efficiently acquire that absolute address, manage linkage, support variable augmented functions, and avoid high overhead for page table entry deletion process as taught by Zucker (col. 4, lines 10-20).

Neither Chen nor Zucker disclose the compiler annotation is an ELF section.

However, Haungs discloses in an analogous computer system the compiler annotation is an ELF section (page 1 of 1, ELF Sections “There are a number of types of sections described by entries in the section header table. Sections can hold executable code, data, dynamic linking information, debugging data (compiler annotations), symbol tables, relocation information, comments, string tables, and notes...” (emphasis added).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of the compiler annotation is an ELF section

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as taught by Haungs into the method of generating binary code file as taught by the combination system of Chen and Zucker. Also, the ELF sections could be many types, and has been known and was originally developed by Unix System Laboratories. The modification would be obvious because of one of ordinary skill in the art would be motivated have the compiler annotation is an ELF section to provide more flexibility to the operating system as suggested by Haungs (page 1 of 2, 1st paragraph).

Per claims 2, 9 and 17:

The rejection of claim 1 is incorporated, and further, Chen disclose:

- wherein the compiler annotation enables binary translation to be performed on the plurality of binary code instructions using a non-heuristic approach (col. 6, lines 17-18 “The translation process... then translates the code into the translated binary objects code”).

Per claims 3, 10 and 18:

The rejection of claim 1 is incorporated, and further, Chen disclose:

- wherein the compiler annotation describes functional characteristics of the plurality of binary code instructions (col. 6, lines 54-58 “the parser processes the sequence of tokens and produces an intermediate level representation, such as a parse tree or sequential intermediate code, and symbol table that records the identifiers used in the program and/or attributes”).

Per claims 5, 12 and 20:

The rejection of claim 1 is incorporated, and further, Chen disclose:

- examining the plurality of source code instructions (col. 6, lines 25-26 “The original source code... is input into the system compiler”);
- reorganizing one or more of the plurality of source code instructions (col. 5, lines 13-18 “The analyzer... checking a program for validity... process takes... intermediate code generated in the parsing... symbol table... determines whether or not the program satisfies the properties required by the source language”);
- translating the plurality of source code instructions into the plurality of binary code instructions (col. 5, lines 47-49 “transforms the code into equivalent machine code in a form of a relocatable... or directly executable object code”);
- reorganizing one or more of the plurality of binary code instructions (col. 6, lines 4-5 “Once the program... compiled... linked to interconnected the parts of the program... needed library routines”); and
- tracking and recording functional characteristics of the plurality of source code instructions and of the plurality of binary code instructions (col. 6, lines 7-8 “The program... routines are read and then relocated by a loader to produce a machine-executable image in memory”).

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Claims 21-23 is the apparatus claim corresponding to method claims 1, 2, and 3 respectively, and rejected under the same rational set forth in connection with the rejection of claims 1, 2, and 3 respectively, above.

Claim 25, 26 is the apparatus claim corresponding to method claims 1, 5 and rejected under the same rational set forth in connection with the rejection of claims 1, 5 above.

Claims 27, 28 and 30 is the apparatus claim corresponding to method claims 2, 3, and 5 respectively, and rejected under the same rational set forth in connection with the rejection of claims 2, 3, and 5 respectively, above.

Claim 28 is the apparatus claim corresponding to method claim 3 and rejected under the same rational set forth in connection with the rejection of claim 3 above.

Claim 31-35 are the computer product claim corresponding to method claims 1-5 respectively, and rejected under the same rational set forth in connection with the rejection of claims 1-5 respectively; above.

Claim 36-40 are the computer product claim corresponding to method claims 1-5 respectively, and rejected under the same rational set forth in connection with the rejection of claims 1-5 respectively, above.

10. Claims 4, 7, 11, 14, 15, 19, 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, Zucker and Haungs in view of US Patent No. 6,353,925 to Stata et al. (hereinafter called Stata).

Per claims 4, 7, 11, 14, 15 and 19:

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The rejection of claim 1, 8, 16 is incorporated, and further, neither Chen nor Zucker nor Haungs explicitly disclose the compiler annotation comprises one or more records selected from a module identification (ID), a function ID, a split function ID, a jump table ID, a function pointer initialization ID, a function address assignment ID, an offset expression ID, a data in the text section ID, a volatile load ID, and an untouchable region ID.

However, Stata discloses in an analogous computer system the compiler annotation comprises one or more records selected from a module identification (ID), a function ID, a split function ID, a jump table ID, a function pointer initialization ID, a function address assignment ID, an offset expression ID, a data in the text section ID, a volatile load ID, and an untouchable region ID (col. 6, lines 40-42 “Each tool... have a set of annotations... recognizes and support... annotations are placed in the source file along with the programming-language statements” and (col. 6, lines 64-66 “the annotation language... say any comment whose first character is the character “@” is an annotation”).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of selecting or having annotations within the code as taught by Stata into the method of generating the binary code files as taught by the combination system of Chen, Zucker and Haungs. The modification would be obvious because of one of ordinary skill in the art would be motivated to use annotations within the code to provide less modification of the code if one need to transfer from one system to another as suggested by Stata (col. 1 and 2, lines 64-67 and 1-6).

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Claim 24 is the apparatus claim corresponding to method claim 4 and rejected under the same rational set forth in connection with the rejection of claim 4 above.

Claim 29 is the apparatus claim corresponding to method claim 4 and rejected under the same rational set forth in connection with the rejection of claim 4 above.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm** Monday to Friday except every other Friday and federal holidays. Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: 571-272-2100**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wei Y. Zhen** can be reached on **(571) 272-3708**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2191


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